AMENDMENTS TO THE CLAIMS

1-5. (Cancelled)

6. (currently amended) A frequency divider configured to provide an output signal having a period equal to a period of a clock signal multiplied by a programmable division ration, the frequency divider comprising:

a plurality of edge-triggered storage elements arranged in at least one loop, wherein each of the elements has a state, and a clock input, and wherein the state of each storage element is determined responsive to a transition of the clock input, the state, or the inverse thereof, of one or more previous elements in the loop, a characteristic of the division ratio, and the previous state, or the inverse thereof, of the element, and the output signal is derived from the state, or the inverse thereof, of at least one of the elements in the loop;

a circuit for determining the number of elements in the loop responsive to the desired division ratio; and

wherein the loop is configured such that there are odd number loop inversions within the loop, the loop inversions are implemented through inverters, and ~~The frequency divider of claim 3 wherein~~ each storage elements is configured to enter a power save mode responsive to assertion of a power control signal.

7. (original) The frequency divider of claim 6 wherein any unused elements are placed in the power save mode through assertion of the power control signal.

8. (currently amended) A frequency divider configured to provide an output signal having a period equal to a period of a clock signal multiplied by a programmable division ration, the frequency divider comprising:

a plurality of edge-triggered storage elements arranged in at least one loop, wherein each of the elements has a state, and a clock input, and wherein the state of each storage element is determined responsive to a transition of the clock input, the state, or the inverse thereof, of one or more previous elements in the loop, a characteristic of the division ratio, and the previous state, or the inverse thereof, of the element, and the output signal is derived from the state, or the inverse thereof, of at least one of the elements in the loop;

a circuit for determining the number of elements in the loop responsive to the desired division ratio; and

wherein the loop is configured such that there are odd number loop inversions within the loop and ~~The frequency divider of claim 2 wherein~~ each storage element comprises a flip-flop coupled to a clock phase module which selectively alters the phase of a clock signal provided to the flip-flop responsive to a control signal indicative of the characteristic of the division ratio, and a data output of the flip-flop.

9. (original) The frequency divider of claim 8 wherein each flip-flop has a master slave configuration.

10. (Cancelled)

11. (currently amended) A method of configuring a programmable frequency divider comprising a plurality of storage elements, each of the storage elements having a data input and a data output, the method comprising the following steps:

obtaining a desired division ratio N;

determining a required number F of storage elements in accordance with the formula:

$$F = \frac{N+P}{2}$$

wherein P is 1 if the desired division ratio is an odd integer, and 0 if the desired division ratio is an even integer;

obtaining F storage elements from the plurality; configuring the F storage elements in a ring arrangement; and

~~The method of claim 10 further comprising~~ placing any unused storage elements in a power save mode.